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QUARTERLY REPORT NO 2
FOR
ANALOG-TO-DIGITAL CONVERTER
Contract No. N00014-87-C-0314
1 July 1987 - 30 September 1987

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Program Code Number: 7220
Name of Contractor: Texas Instruments Incorporated
13500 N. Central Expressway
P. O. Box 655936, M. S. 105
Dallas, Texas 75265
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Contract Period Covered by Report: 1 July 1987 - 30 September 1987

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QUARTERLY REPORT NO. 2
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ANALOG-TO-DIGITAL CONVERTER
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I. SUMMARY

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A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter and a high resolution GaAs A/D converter.

B. Baseline Process Development

A new process development test chip was designed during the first quarter of this program. During the second quarter, the mask set was used to develop a baseline process. Eight lots were processed to determine the impact of the base doping and epitaxial profile on the transistor dc parameters such as gain, leakage currents, and breakdown voltages. A first-pass baseline process has been developed that yields suitable current gains and breakdown voltages, but results in low Early voltages. Future efforts will be aimed at improving the Early voltage by lowering the collector doping levels and increasing the base doping level.

C. Advanced Process Development

Advanced process development is proceeding on two fronts. The first will evaluate materials-related issues using an overgrowth process to obtain the proper doping profiles. Toward that end, two overgrowth lots have been successfully completed. Both lots yielded wafers with good HBTs, demonstrating the feasibility of our approach, which utilizes MOCVD for both the initial epi growth and the overgrowth. Transistors were fabricated with current gains as high as 1000, indicating a high quality interface between the initial epi and the overgrowth layer.

The use of self-aligned HBTs represents our second major effort toward fabricating a high speed ADC and is fully compatible with the overgrowth

process. The self-aligned HBT development effort will intensify as progress is made on the baseline process.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

A. Baseline Process Development

Eight baseline process lots have been completed in an effort to evaluate the impact of the key process parameters. These parameters, which include the base doping profile, emitter doping profile, and grading of the HBT AlGaAs emitter at the base-emitter junction, were varied in a systematic manner. The resulting transistor parameters have been partially characterized. The impact on the common emitter current gain (H_{fe}) of these parameters is illustrated in Figure 1, where the average H_{fe} and standard deviations for each wafer are plotted versus the calculated integral of the base dopant or Gummel number. The base Gummel number was controlled by varying the beryllium implant energy and/or dose, as well as by changing the thickness of the emitter layer. The H_{fe} values for different wafers fabricated with epi from the same MOCVD epitaxial deposition run are plotted using the same symbol and are connected by straight lines.

These results show that the current gains for wafers from the same epitaxial run and different base Gummel numbers all lie on essentially parallel lines, with the current gain varying inversely with the base Gummel number as would be expected. In addition, the current gain for a given base Gummel number is strongly dependent on the epitaxial emitter grading profiles. Epi runs 13 and 14 were designed to yield a 300 Å graded bandgap AlGaAs emitter layer at the emitter-base (e-b) interface while maintaining a constant emitter doping density. Epi run 15 was similar to 13 and 14 with the addition of a 100 Å undoped buffer layer at the e-b interface. Epi run 16 was similar to 13, except that the AlGaAs emitter thickness was increased by 600 Å. Epi run 18, in which the grading of the AlGaAs layer extended into the base region, resulted in the lowest gains. The remaining epitaxial runs yielded profiles with similar variations. On the basis of these results, the epitaxial process utilized in runs 13 and 14 was selected as our baseline process.

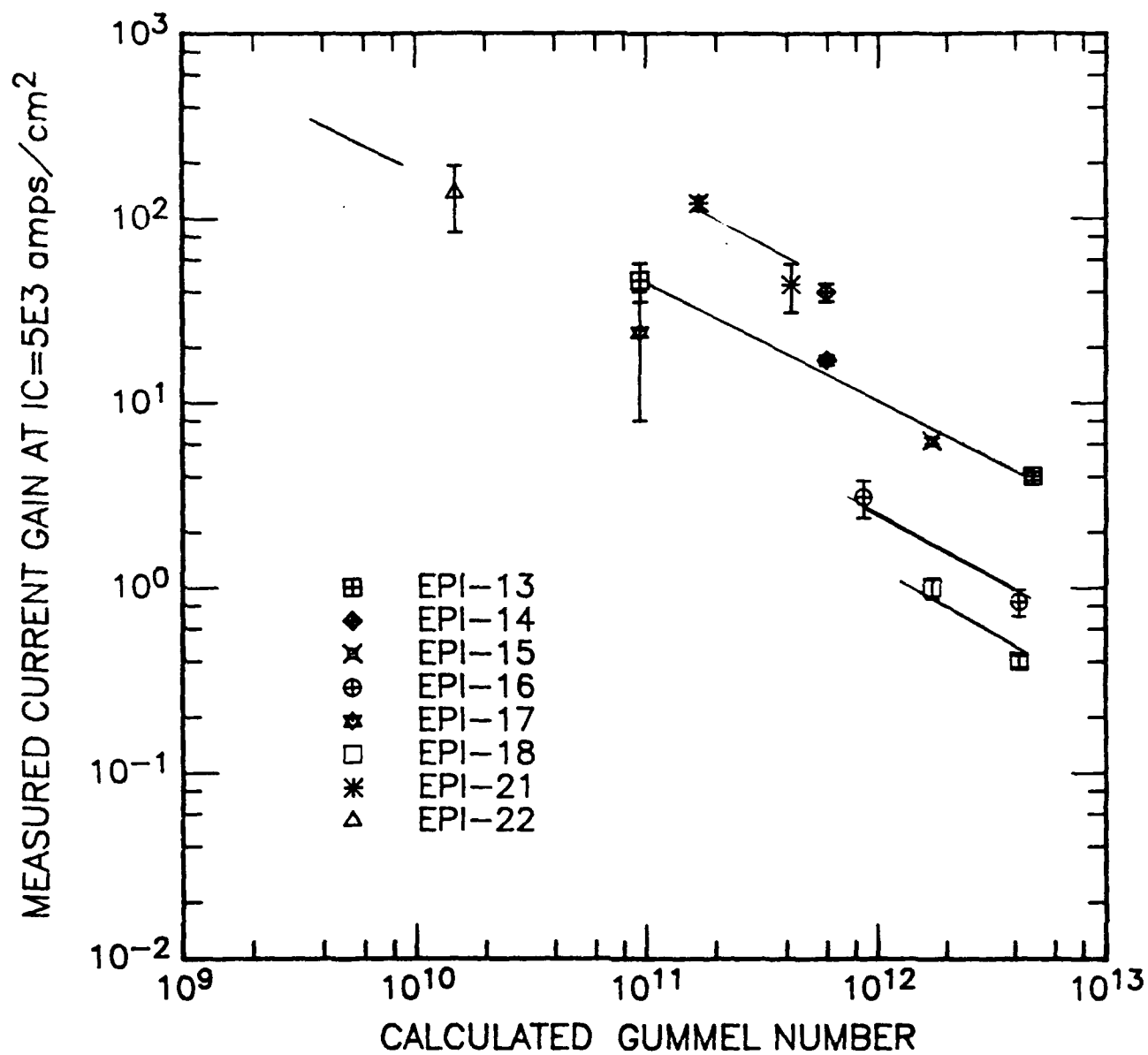


Figure 1. Current gain (H_{FE}) vs Gummel number.

Figure 1 shows that low base dopant levels must be used to increase the current gain. This impacts device performance in several areas. One is an increase in the base resistance; another is a reduction in the collector-emitter punchthrough voltage. This latter effect is illustrated in Figure 2, which shows the wafer average punchthrough voltage versus the base Gummel number. These breakdown voltage data indicate the minimum base Gummel number is in the range of $5.0 \times 10^{11}/\text{cm}^2$. This would set an upper limit on the current gain of about 60. Low punchthrough voltages are accompanied by low Early voltages and low output resistances, as shown in Figure 3, which illustrates the I-V characteristics of an HBT. It can be seen that although the transistor gains are greater than 200, the output characteristics have a significant slope, which results in a low output resistance and an Early voltage of approximately 0.6 V.

To address the problem associated with the coupling between the current gain and the punchthrough voltage, we are investigating two approaches. The initial solution will be to reduce the collector doping level from 5.0×10^{16} to 2.0×10^{16} per cm^3 to increase the fraction of the applied voltage that is dropped across the collector space-charge region, and thereby increase the base punchthrough voltage. The long-range solution is to use the overgrowth process, as discussed below in Section II.B.

B. Advanced Process Development

Two wafers from the first implanted-base MOCVD overgrowth lots, 19 and 20, have been processed up to first-level metal. The slice with the AlGaAs sacrificial layer and poor morphology had $7 \times 7 \mu\text{m}$ transistors with an average current gain of 23 at $5 \times 10^3 \text{ A}/\text{cm}^2$. The slice with the nitride sacrificial layer and good morphology had a shallow implanted base and a low Gummel number, resulting in high gain, ~ 1000 , with a low $B_{V_{CE0}}$, $\sim 0.5 \text{ V}$. This gain of 1000 demonstrates low recombination at the overgrowth interface and a good overgrowth process. Figure 4 compares the I-V characteristics of a transistor from the wafer with the AlGaAs sacrificial layer and the I-V characteristics of a transistor from the baseline process in which the base is implanted through the emitter. Both transistors exhibit good current gain, while the overgrowth transistor exhibits a higher output resistance and Early voltage.

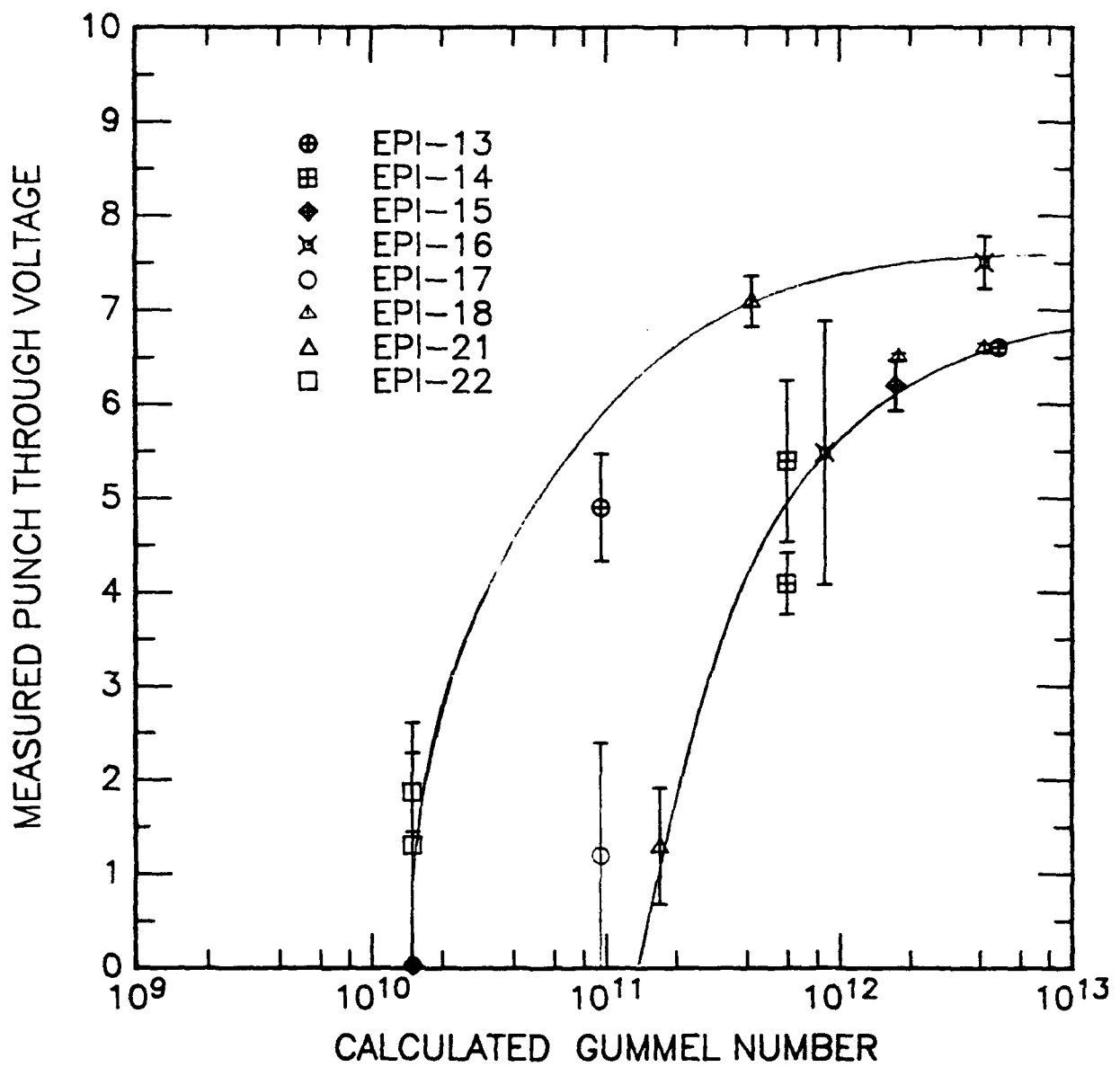


Figure 2. Punchthrough voltage vs Gummel number.

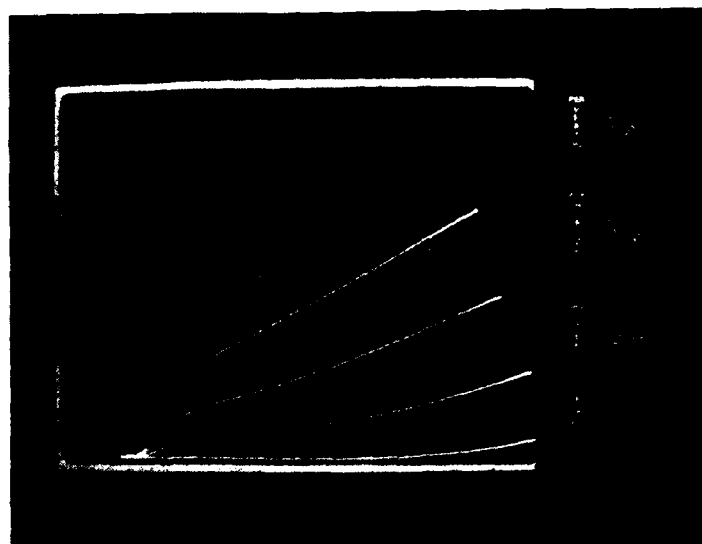
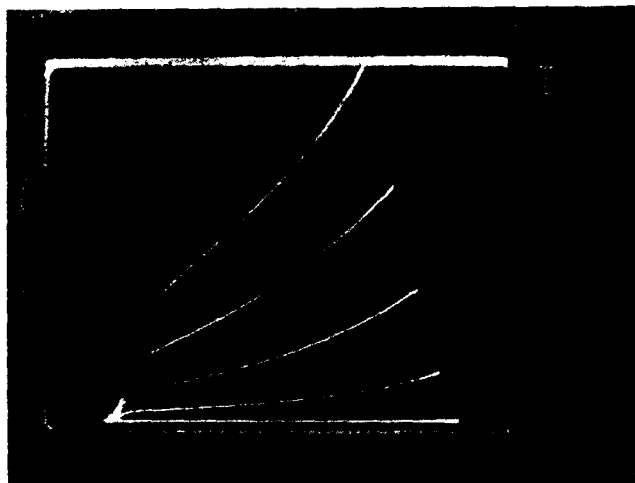
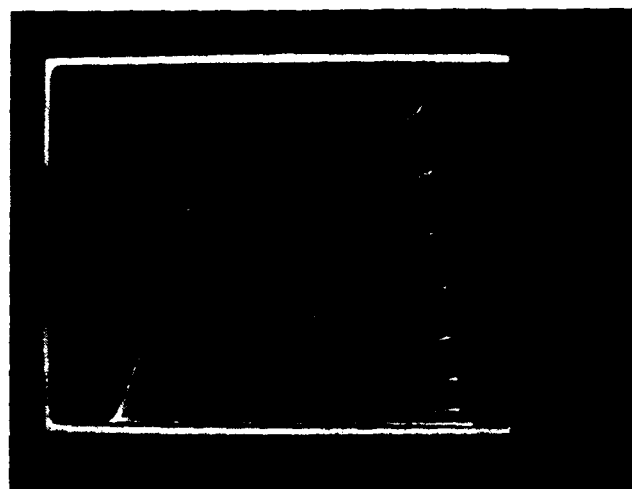


Figure 3. HBT I-V characteristics illustrating high current gains and low output resistance and Early voltage.

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Selective Base Implant Through
AlGaAs Emitter



Selective Base Implant Followed
by AlGaAs Overgrowth

Figure 4. Typical I-V characteristics of planar HBT.

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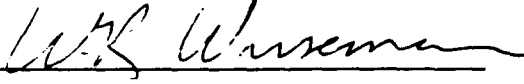
The two additional lots of implanted base overgrowth material, lots 29 and 30 (five wafers in each lot), are at p^+ implant after the second epi deposition. The surface morphology of lot 29 (silicon nitride as the sacrificial layer) is excellent, while lot 28 (AlGaAs as the sacrificial layer) shows numerous defects. Removing the AlGaAs sacrificial layer causes defects in the first epi that propagate into the second epi. This defect production is probably related to inadequate Al oxide removal in the AlGaAs layer, which results in some oxide remaining at the interface. If the silicon nitride sacrificial layer proves adequate for interface protection and base passivation during the first epi processing, then the AlGaAs effort will be dropped.

The alternate overgrowth approach uses a grown base layer selectively etched, followed by a second epi emitter overgrowth. Four lots, five wafers each in first epi runs (runs 31, 32, 36, and 37), will examine the base/emitter interface. These first epi runs have the same 1000 Å, $1 \times 10^{19}/\text{cm}^3$, Zn-doped base, while a spacer layer, ~150 Å, on top of the base is varied from an undoped layer (runs 31 and 36) to an n^+ GaAs layer (run 32). First epi run 37 does not have a spacer layer. The lots processed out of these first epi runs will have the same second epi, which helps to pinpoint the effect of the spacer layer. Lot 3132AB, the A and B wafers out of epi runs 31 and 32, is at p^+ base contact implant after a second epi deposition that looks good. Lot 3132CD is at the second epi deposition. Lot 3637AB is at clean-up prior to second epi, and lot 3637CD is at alignment mark definition in the first epi.

III. ANALOG-TO-DIGITAL CIRCUIT DEVELOPMENT

During the past quarter, Hughes personnel received a copy of the TI test mask database and have successfully converted it to their Calma and Mentor workstations. The layout and design of the test devices have been reviewed by their circuit designers. This review identified a number of device design issues, i.e., naming conventions, layout rules, and design philosophy, that need further clarification. These topics will be discussed during the October TI/Hughes meeting at Hughes.

Hughes has also received wafers from four process lots for their ac and dc characterization.


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